Advanced Algorithms and Techniques for Resilient Time Provision

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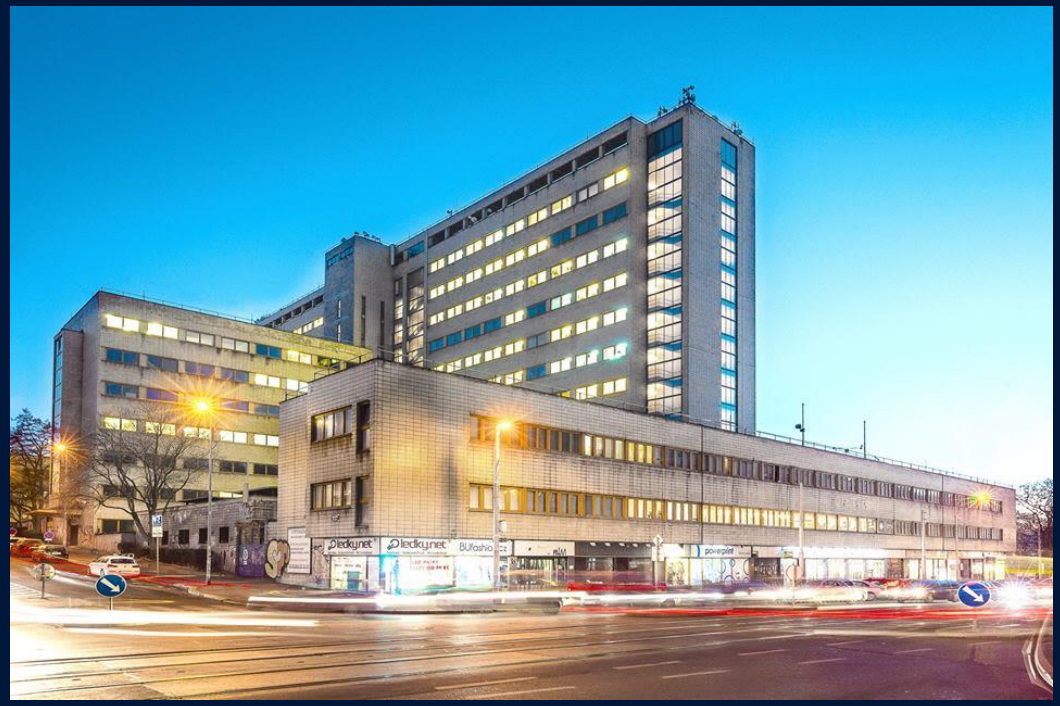
Huld Czech

- Founded in 2015 as Space System Czech
- Transformed to HULD in 2020
- Headquarter in Prague center:
  Nám.Winstona Churchilla 1800/2

- About 20 Employees

- ISO 9001 certified
- ESA financial audit 09/2022
- ESA business code 8000007731



Flight Software development

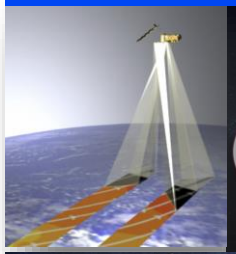
Protocols: CSP, PUS-C, CAN, MIL-STD1553B,
Standards: ECSS, CCSDS, MISRA-C, IEC 65108, EN5010
Languages: C, C++, ADA, Java, Python

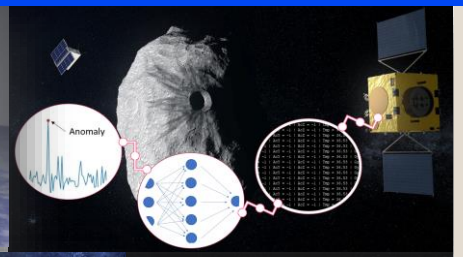
Design & development of safety-Critical software according to the ECSS standards, experience with Software Criticality B, C. Central Software & Application Software.

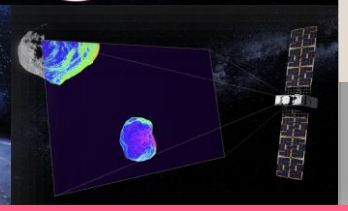
Quantum technologies

Technologies: Quantum computers, Quantum algorithms, Qiskit, PQC, Image processing,

- Space debris collection optimization
- Post-quantum cryptography
- Quantum-based space data processing







Technology development

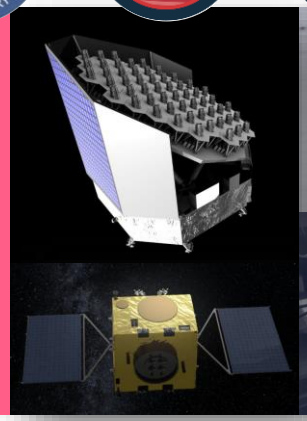
Technologies:
GNSS, AI/ M&L, Kalman filtering, data fusion, FPGA

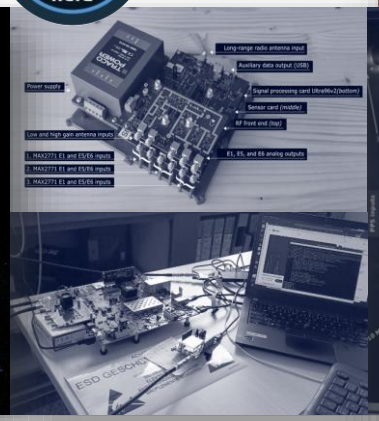
- Anti-spoofing and jamming solution
- Resilient Time Provision platform
- Platform for Cooperative positioning

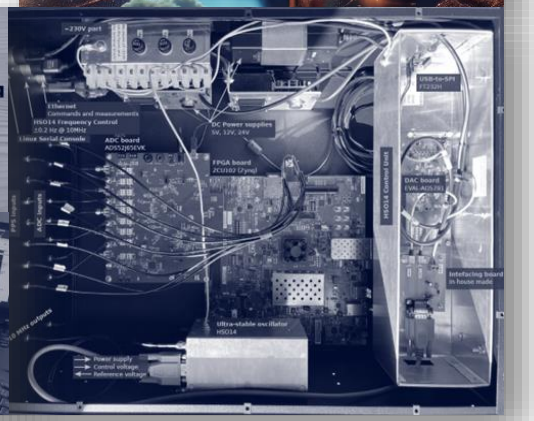
Validation and Verification

Standards: ECSS, CCSDS, MISRA-C, IEC 65108, EN5010

(Independent) Validation and Verification of safety-critical software, including development of Software Validation Facilities.







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Universtity Of West Bohemia in Pilsen

- Founded in 1991 by merging College of Mechanical and Electrical Engineering, and the Faculty of Education (both schools with a forty-year tradition)
- Currently 9 faculties, 62 departments, 130 study programmes
- 12 thousand students
- Modern university campus and research centres of excellence

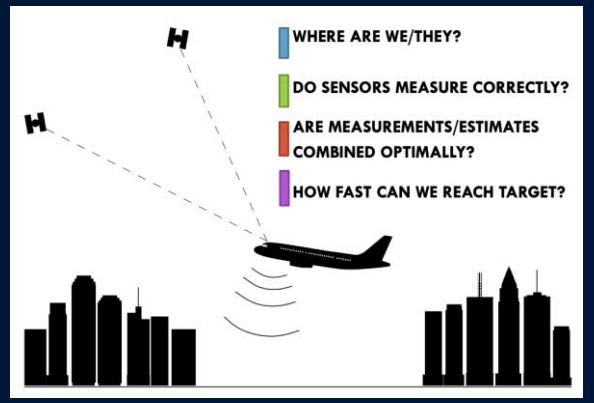
Identification and Decision Making Research Group

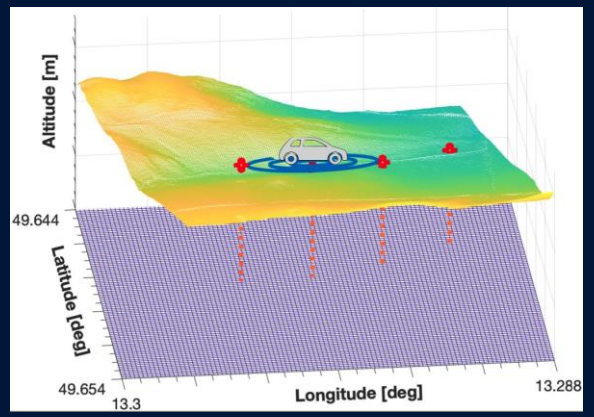
- Department of Cybernetics, Faculty of Applied Sciences

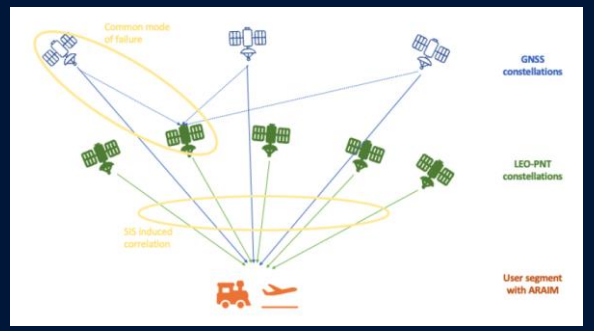
- **Research Interest**: State estimation, navigation, fault detection, control, system identification and fusion
- **Publications** 2020-2024: 20+ journal papers, 70+ conference papers (IEEE, IFAC, ISIF, ION)

- **Funding**:
  - Office of Naval Research, Airfroce Reseach Laboratory, European Space Agency, EU Horizont
  - Czech Science Foundation, Technology Agency of the Czech Republic

- **Applications**: RAIM algorithms for GNSS-based localization of trains, Attitude and heading reference system, Terrain-aided navigation, Navigation sensor design, Precize time provision







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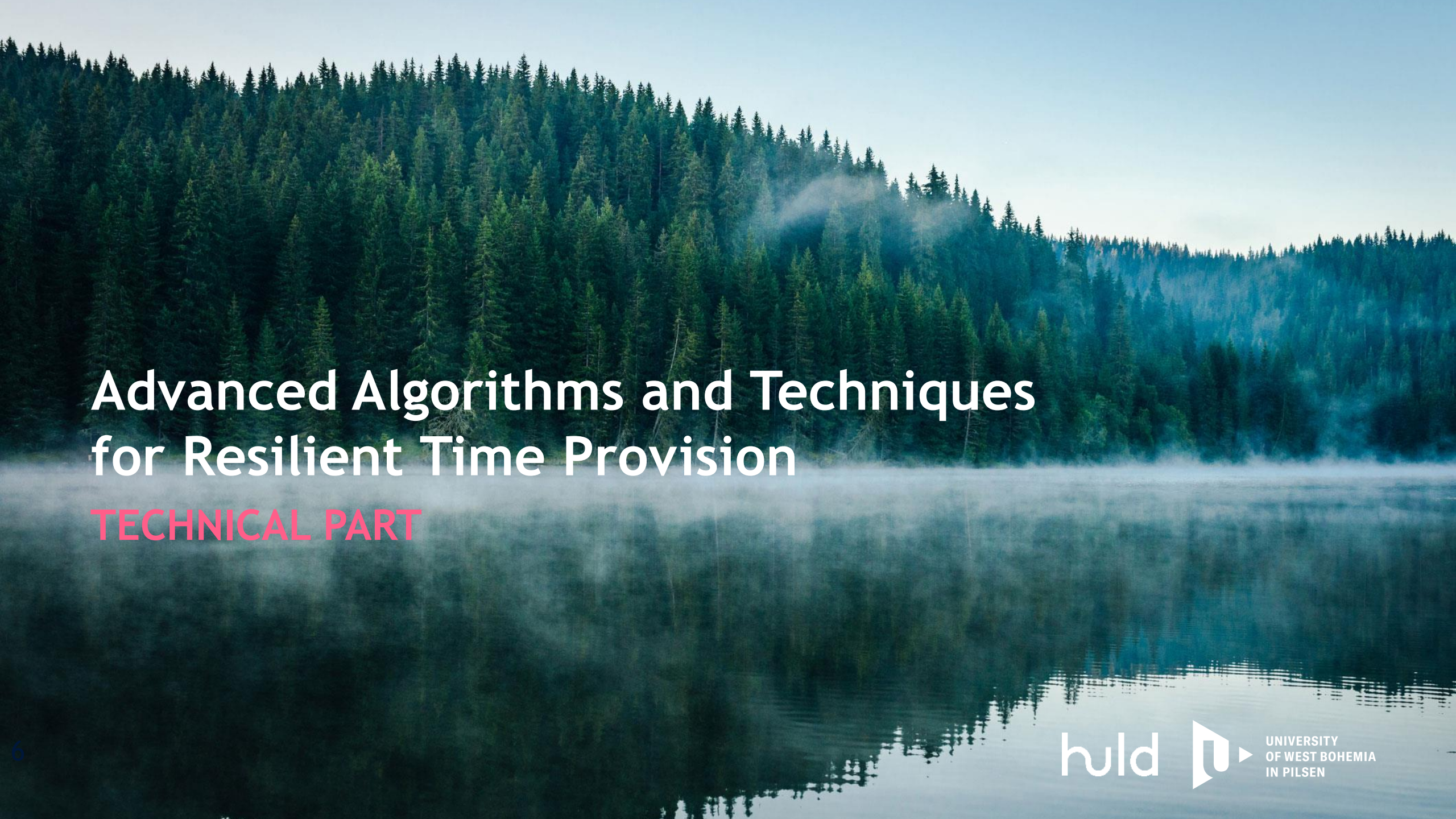

Advanced Algorithms and Techniques for Resilient Time Provision

TECHNICAL PART

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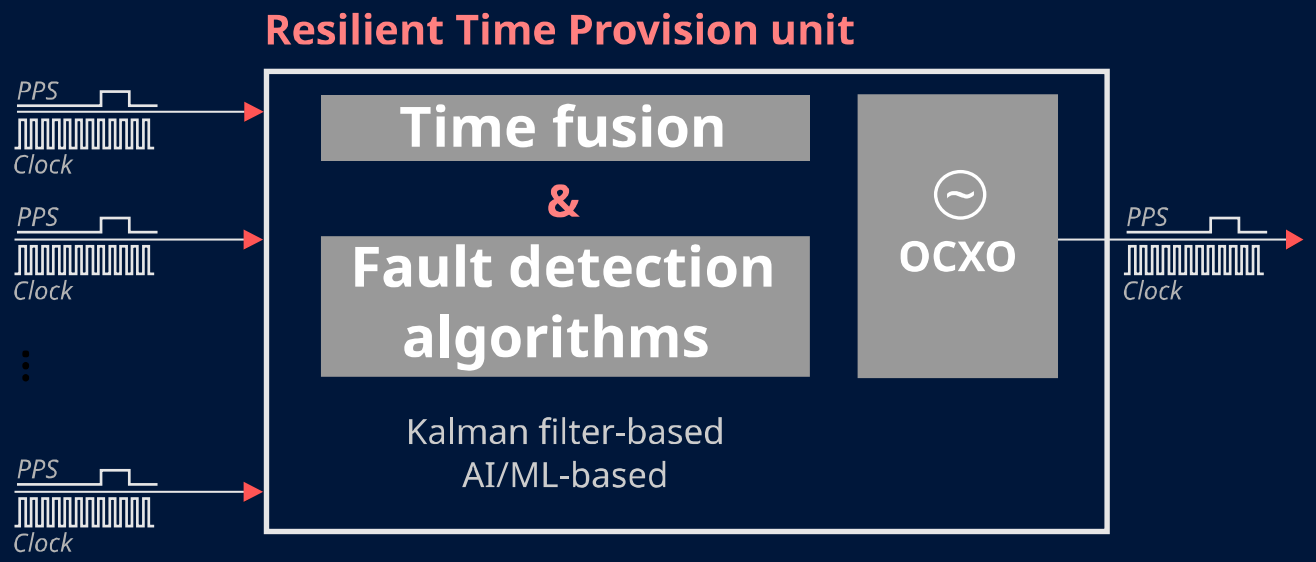
Content

- Project overview
- Project summary
- Market survey
- Use cases
- Requirements
- Measurement techniques
- System overview
- Hardware
- Software
- Algorithms
- Verification examples
- Future improvements
- Conclusion

Project overview

- Develop a system generating accurate and stable timing information with high level of integrity

- Combine the timing information provided by several timing sources and create output timing information with superior characteristic
- Detect inconsistencies among the inputs and exclude the faulty inputs from the clock combination product



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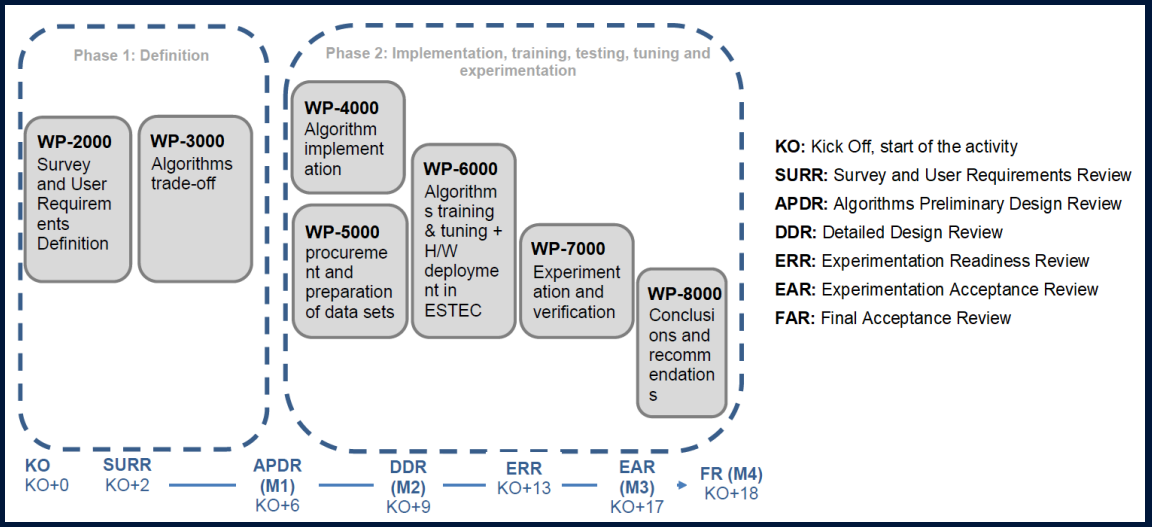
Project summary

- NAVISP Element 1, NAVISP-EL1-056,
- Huld s.r.o. as the prime contractor, UWB as the subcontractor
- Duration 18 months
- Kick-off meeting on 01.09.2022
- Work packages (WP):
  - WP-2000: Survey & User requirements definition
  - WP-3000: Algorithms trade-off & pre-prototyping
  - WP-4000: Algorithm implementation
  - WP-5000: HW prototypes & data sets preparation
  - WP-6000: Algorithms training and tuning & HW deployment
  - WP-7000: Experimentation & verification



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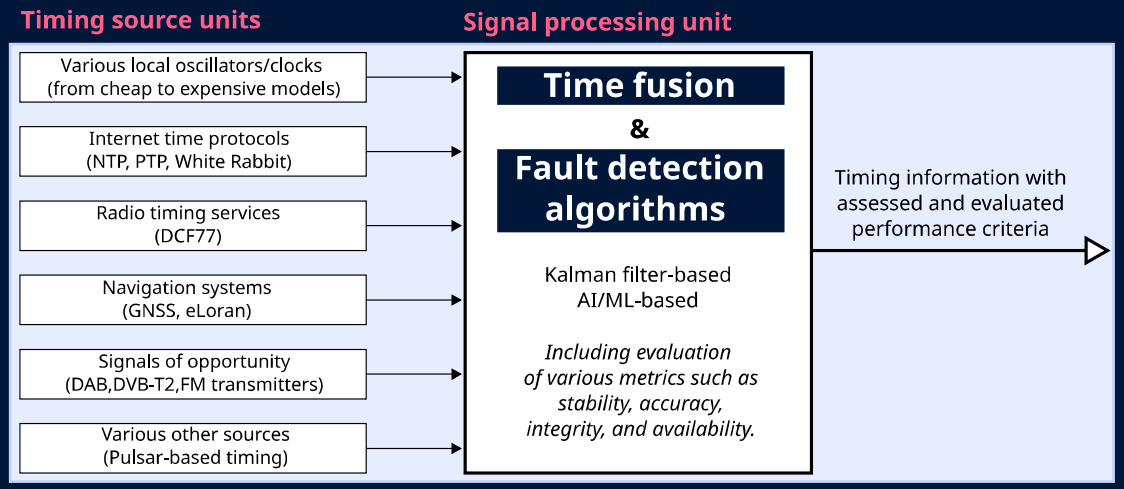
Market survey

- Focusing on: *Accuracy*, *availability*, and *continuity*
- Examined areas and summary:
  - Finance: Maximal divergence from UTC equal to 100 us and the resolution of timestamps of 1 us.
  - Power grids: Expected accuracy in near future 0.05 us to 0.3 us.
  - Oil and gas infrastructure: Information about required timing accuracy was not found. We suppose that accuracy as provided by NTP is sufficient with a significant margin for this market.
  - Telecommunications: Expected 10 ns for high accuracy location service in 5G networks.
  - Transport: Since 5G is supposed to be an enabler for the autonomous driving concept, the timing accuracy is derived from 5G, hence at the level of 10 ns.
  - Scientific applications: Sub-ns accuracy of synchronization of more than 1000 nodes via fiber or copper connections of up to 10 km of length (White Rabbit).
  - Metrological laboratories: Accuracy in range of ns is required for time-wise synchronization of distant timing laboratories. Recently reported accuracy of synchronization system operating over 50 km long fiber optical link is in range of a few ps.
  - Availability: 99.999%
  - Continuity: 30 years

Use cases

- Commercial solution
  - Targeting various critical infrastructures
  - A critical infrastructure of common markets typically consists of
    - An underlying data network, allowing time transfer over various protocols, typically NTP or PTP, and
    - GNSS receivers geographically spread around the network, providing the time reference to NTP/PTP.
- High-end solution
  - Time synchronization of distant places
    - However, this use case seems to be well covered by already available solutions such as White Rabbit (possibly over optical link), and synchronization of distant place by means of GNSS.
    - Thus, we do not anticipate competing in this area.
  - Comparison of various high stable atomic clocks
- High-end solution > Commercial solution



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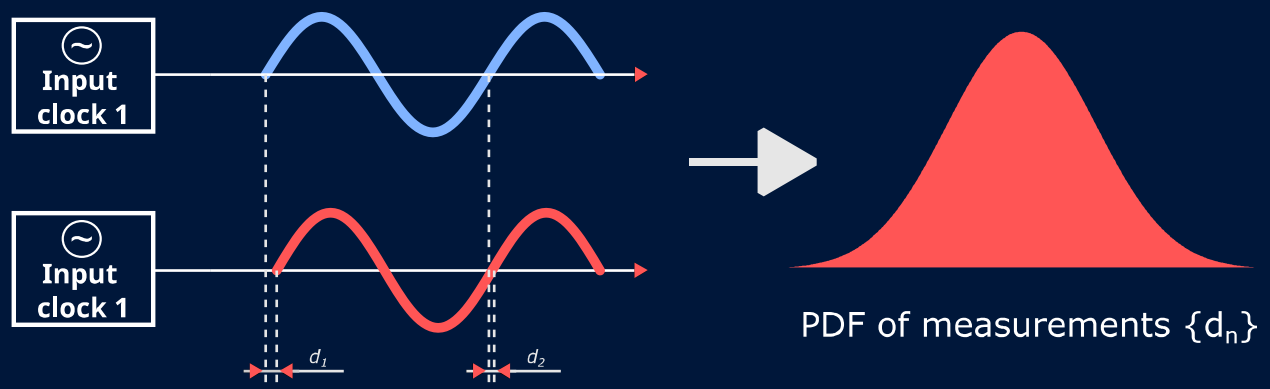
Requirements

- Two sets of requirements: Commercial and High-end solutions
- Common main requirements:
  - 4 algorithms for clock combination
  - Clock combination product (the ensemble) shall be used to steer the output physical clock signal
  - 4 algorithms for fault detections
    - 2 of them shall exploit machine learning
- Accuracy:
  - Commercial solution better than 10 ns
  - High-end solution better than 0.1 ps



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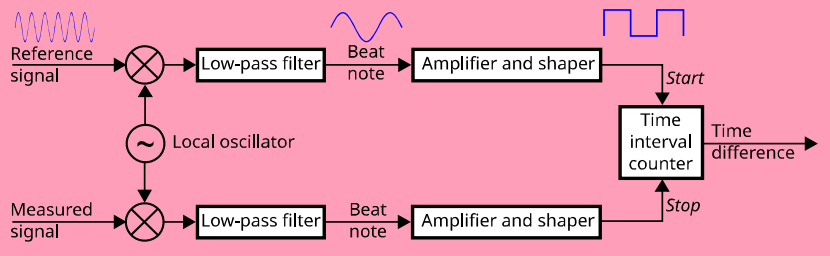
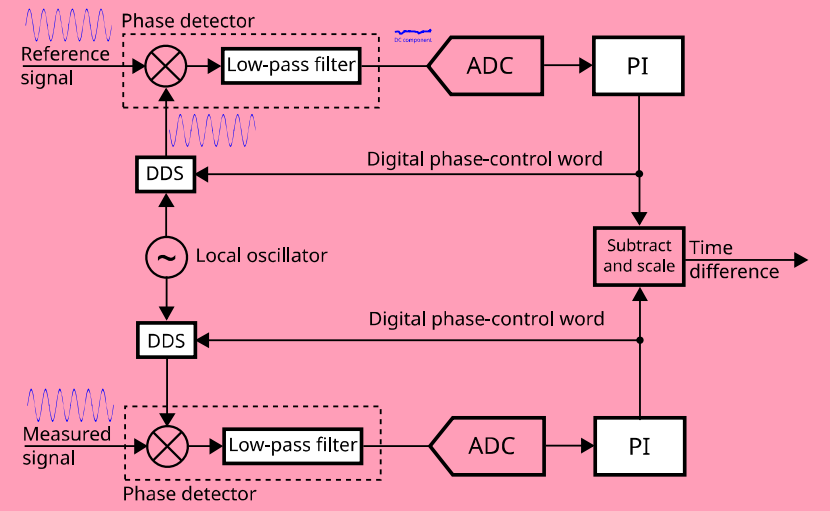
Measurement techniques

- **High Frequency Signals**
  - Methods
    - Dual Mixer Time Difference (DMTD)
    - Tracking Direct Digital Synthesizer (TDDS)
  - Performance in terms of Allan deviation (ADEV)
    - DMTD based on
      - N210 SDR (14-bit ADC), 2016, [1]: ADEV 3 x 10^{-14} at 1 s
      - N210 SDR (14-bit ADC), 2018, [2]: ADEV 6 x 10^{-14} at 1 s
      - B210 SDR (12-bit ADC), 2019, [3]: ADEV 2 x 10^{-14} at 1 s
    - TDDS, 2018, [4]: ADEV 1.5 x 10^{-14} at 1 s
    - For reference purpose only: Commercially available Phase noise analyzer 53100A (Microchip, [5]) achieves ADEV 5 x 10^{-14} at 1 s
  - We selected DMTD implemented fully in the baseband
    - Considering the complex signals (rather than the real signals shown in the diagram)
    - Time interval counter is not necessary



Dual Mixer Time Difference (DMTD)



Tracking Direct Digital Synthesizer (TDDS)

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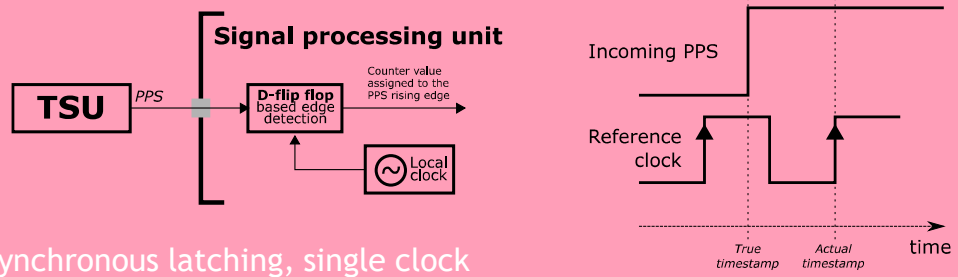
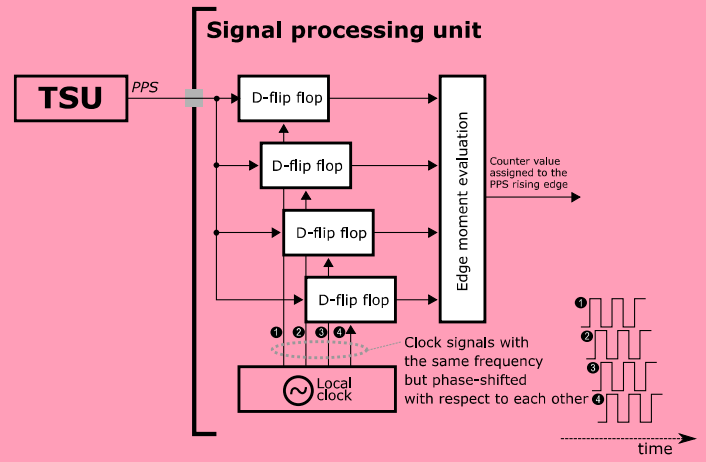
Measurement techniques

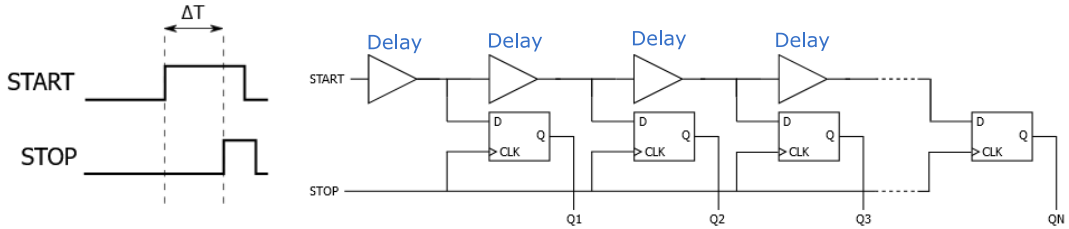
- **Pulse per second (PPS)**
  - Methods
    - FPGA based
      - PPS edge latching, single clock
        - Resolution given by the clock period
      - PPS edge latching, phase-shifted clocks
        - Resolution given by the fraction of the clock period
      - Time to digital converter (TDC)
        - Accuracy given by the FPGA technology
        - Open source TDC [6] reports 52 ps resolution with 95% confidence
    - ADC based [2]: Standard deviation 16.6 ps
    - IC based: TDC7200 (Texas Instruments):
      - Resolution 55 ps
      - Standard deviation 35 ps
  - We selected FPGA-based TDC



Synchronous latching, single clock



Synchronous latching, phase-shifted clocks



Time to digital converter (TDC)

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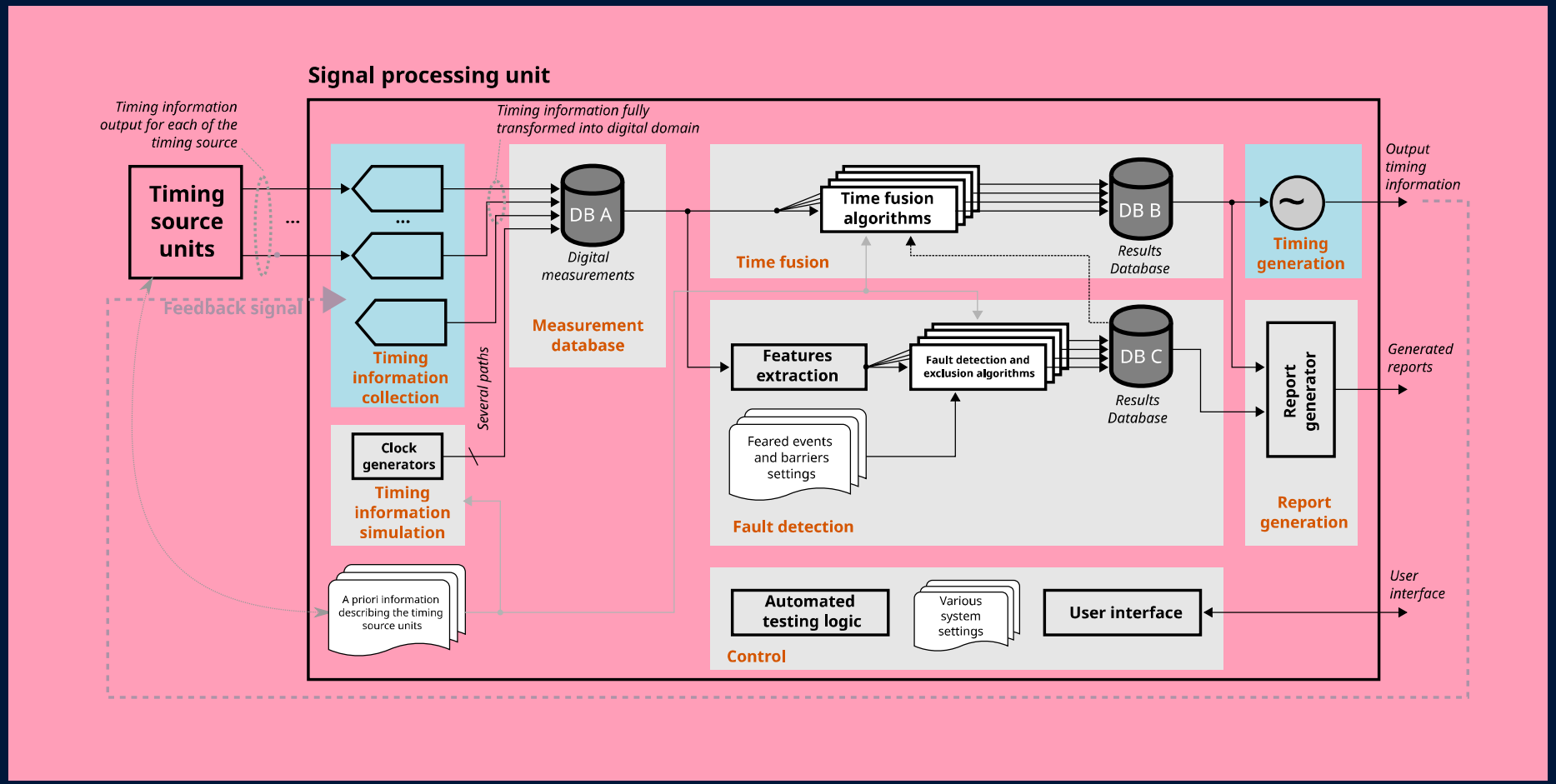
System overview



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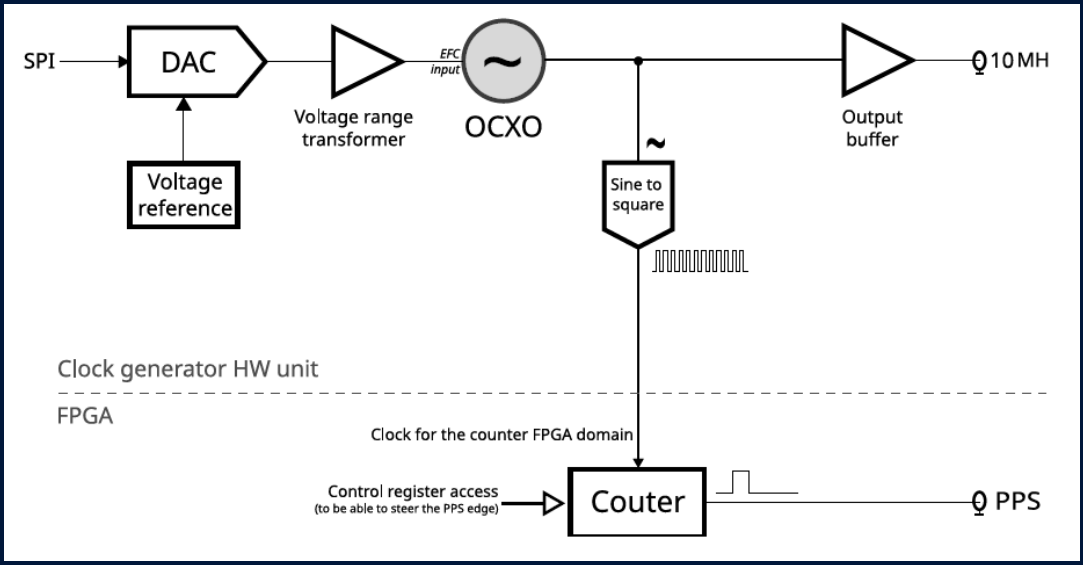
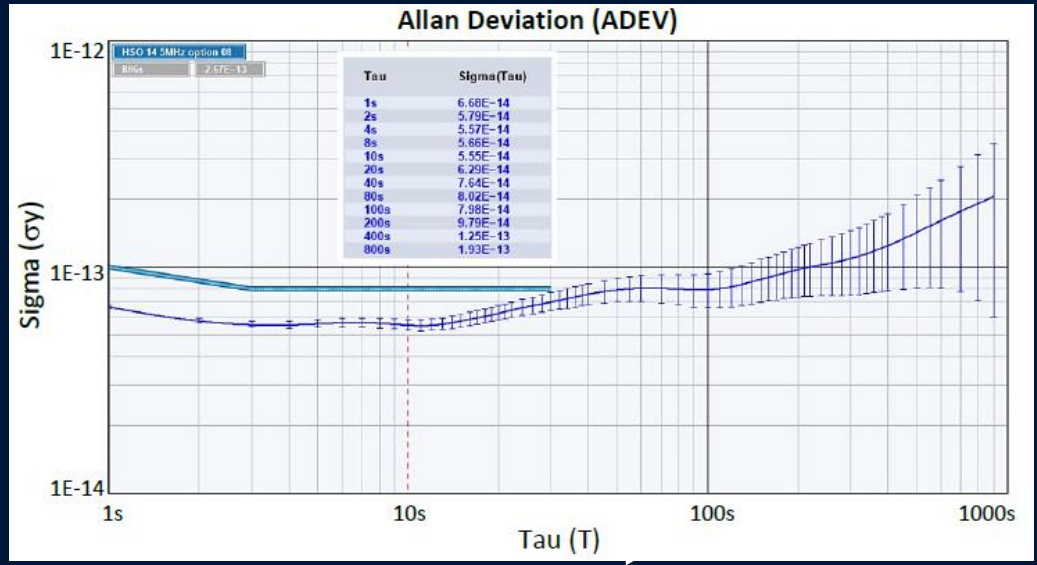
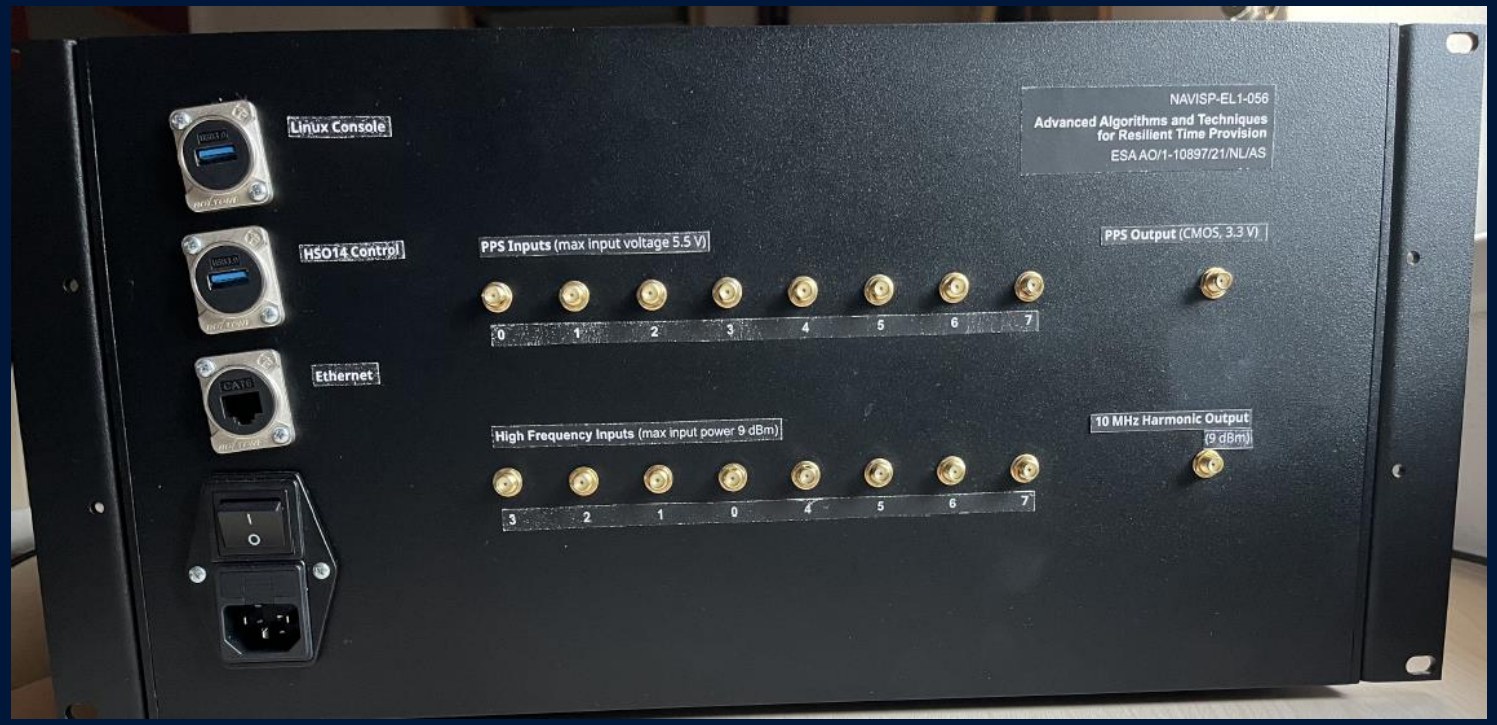
Hardware

- ADC
  - ADS52J65 (Texas Instruments): 8 channel, 16-bit resolution, 125 MHz sampling rate, JESD204B interface
- System on the Chip
  - Zynq UltraScale+ XCZU9EG-2FFVB1156 on ZCU102 evaluation kit (AMD / Xilinx)
- Local clock
  - Based on HSO14 (Rakon)





Hardware



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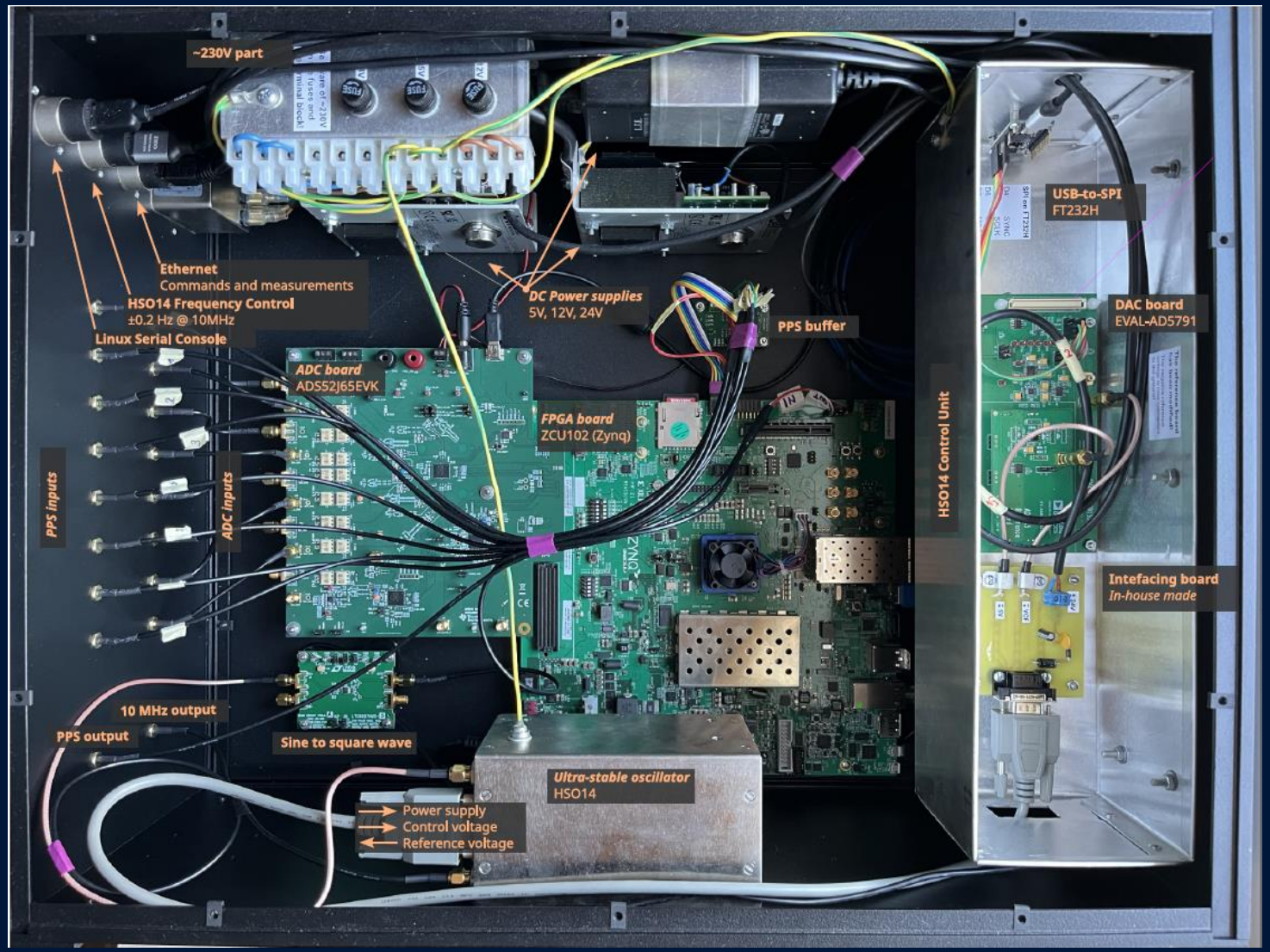
Hardware



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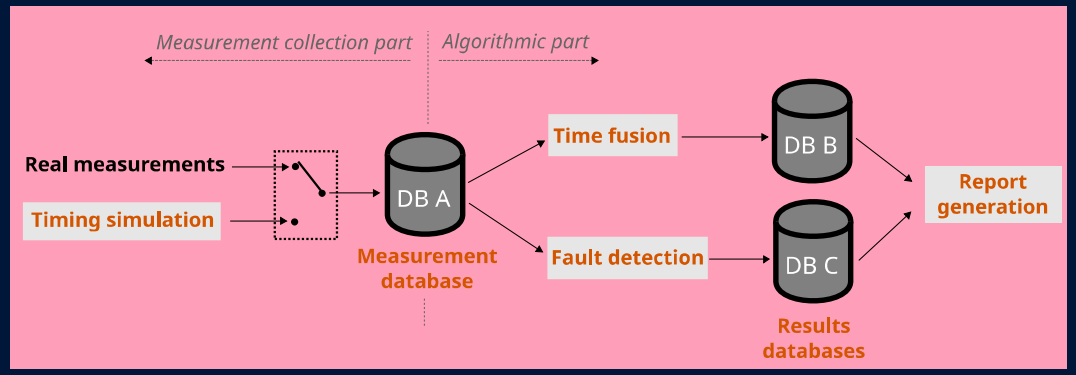
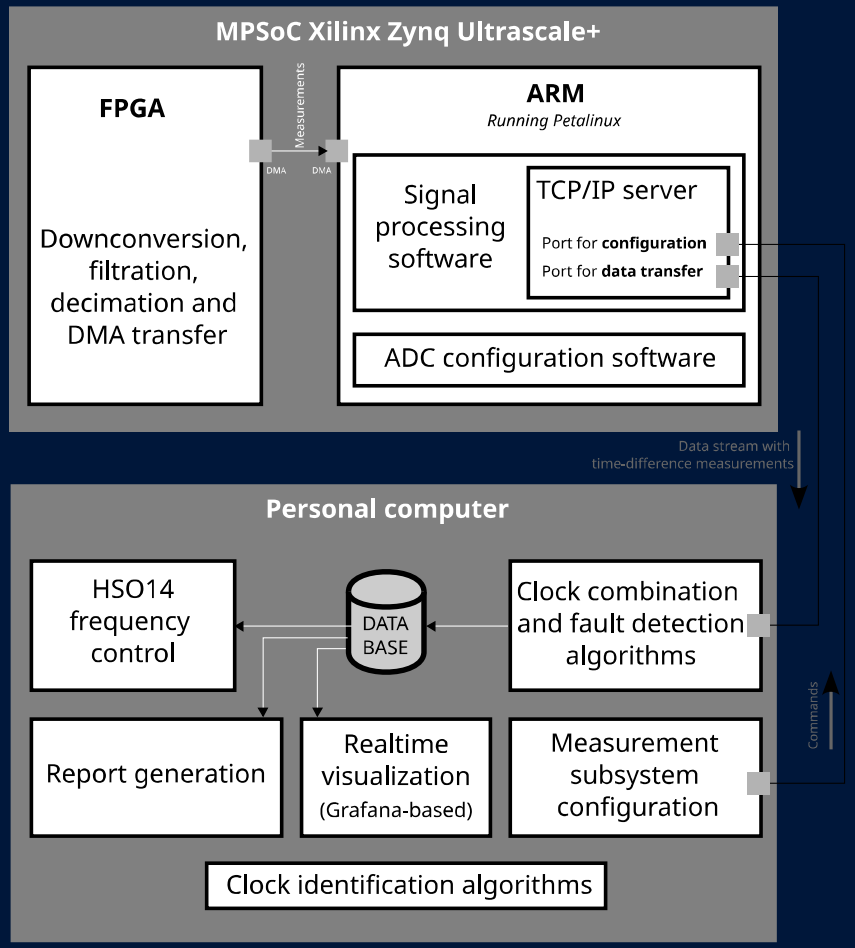
Software

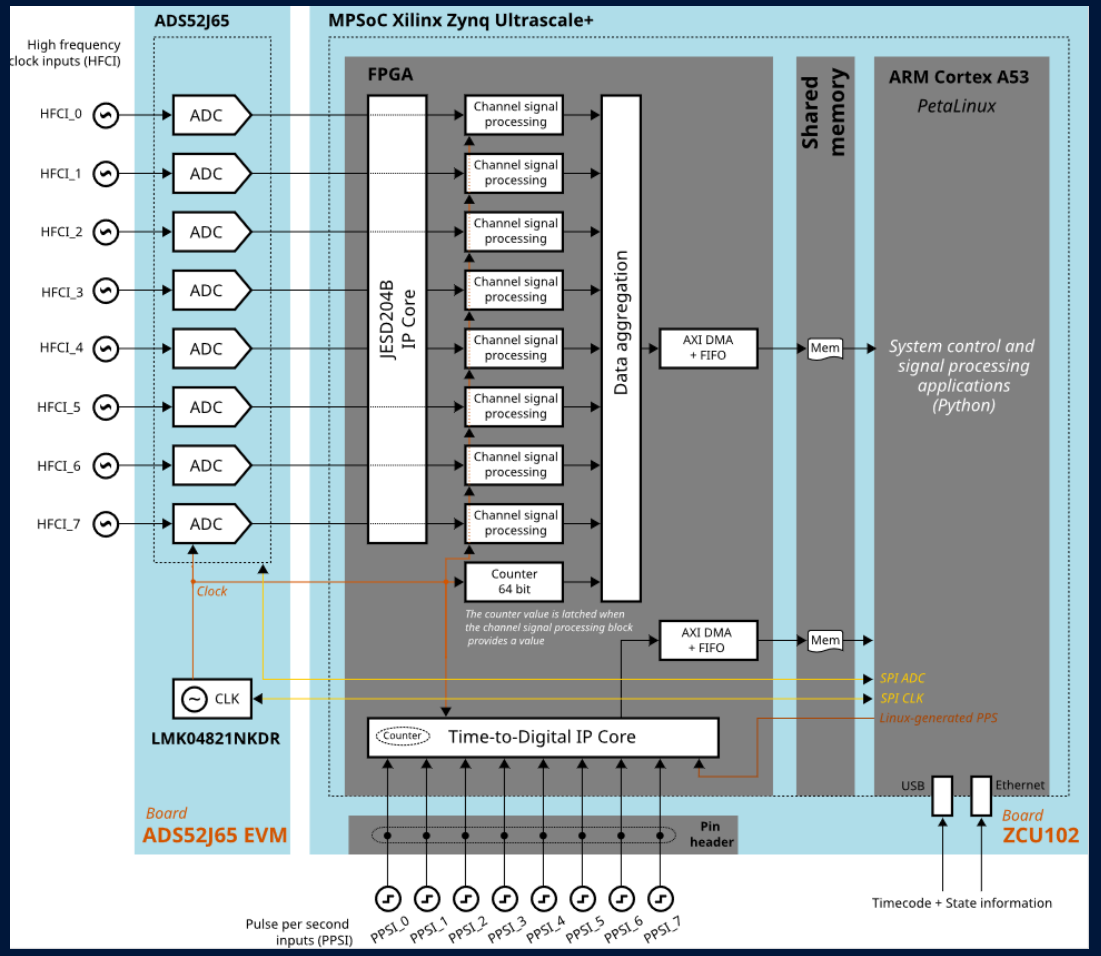
- High level architecture
  - Low-level part: The measurement collection part
  - High-level part: The algorithmic part
- Design choices
  - Matlab/Python for the prototyping of the algorithms
  - Python for high-level software
  - InfluxDB as the database
  - Grafana as the real-time visualization tool
  - C for low-level software
  - VHDL for FPGA firmware
  - PetaLinux as the operating system for the embedded system part
  - Debian GNU/Linux as the operating system for the control computer



Software



Software architecture



FPGA firmware architecture

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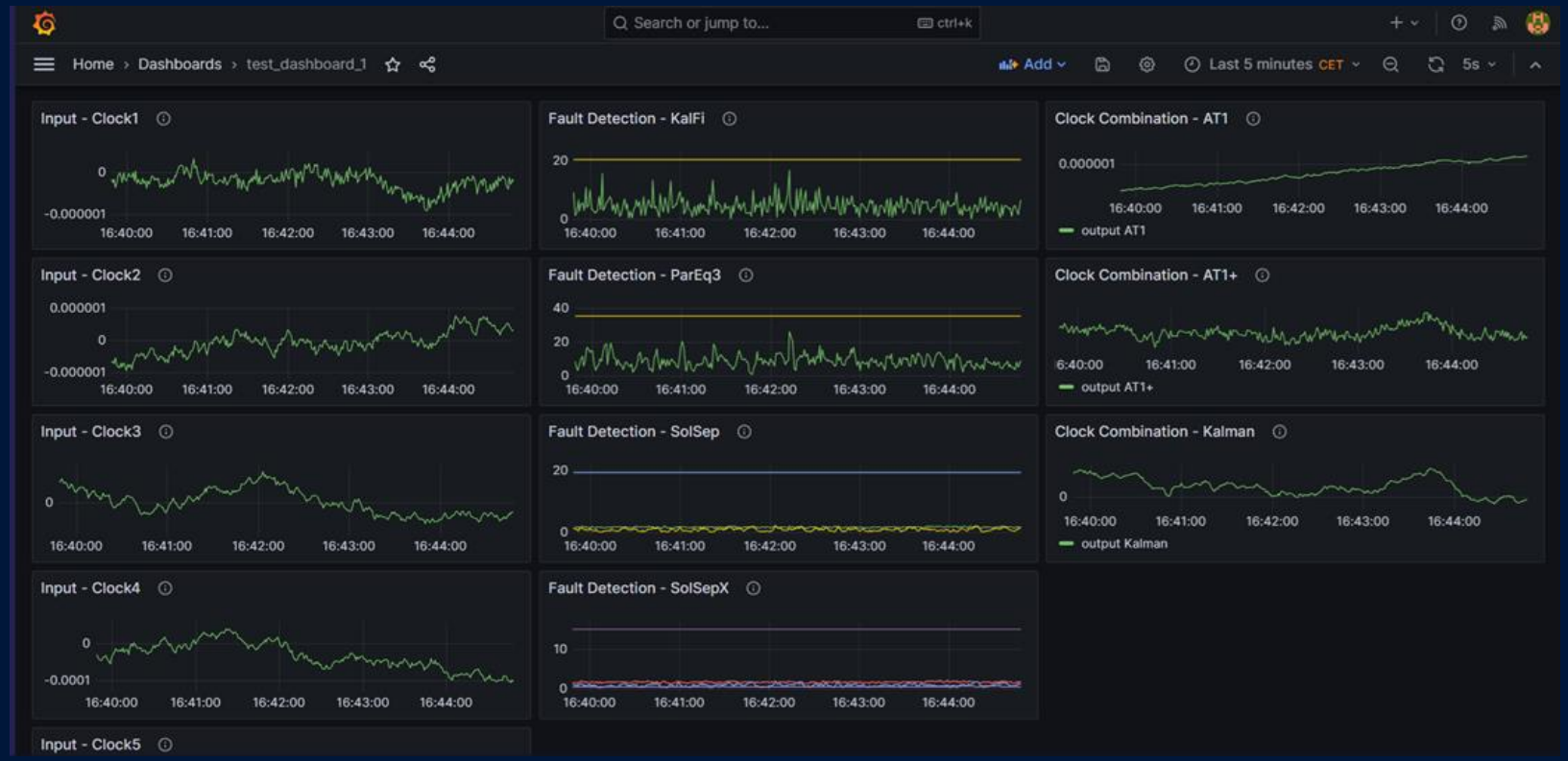
Software

- Visualization example



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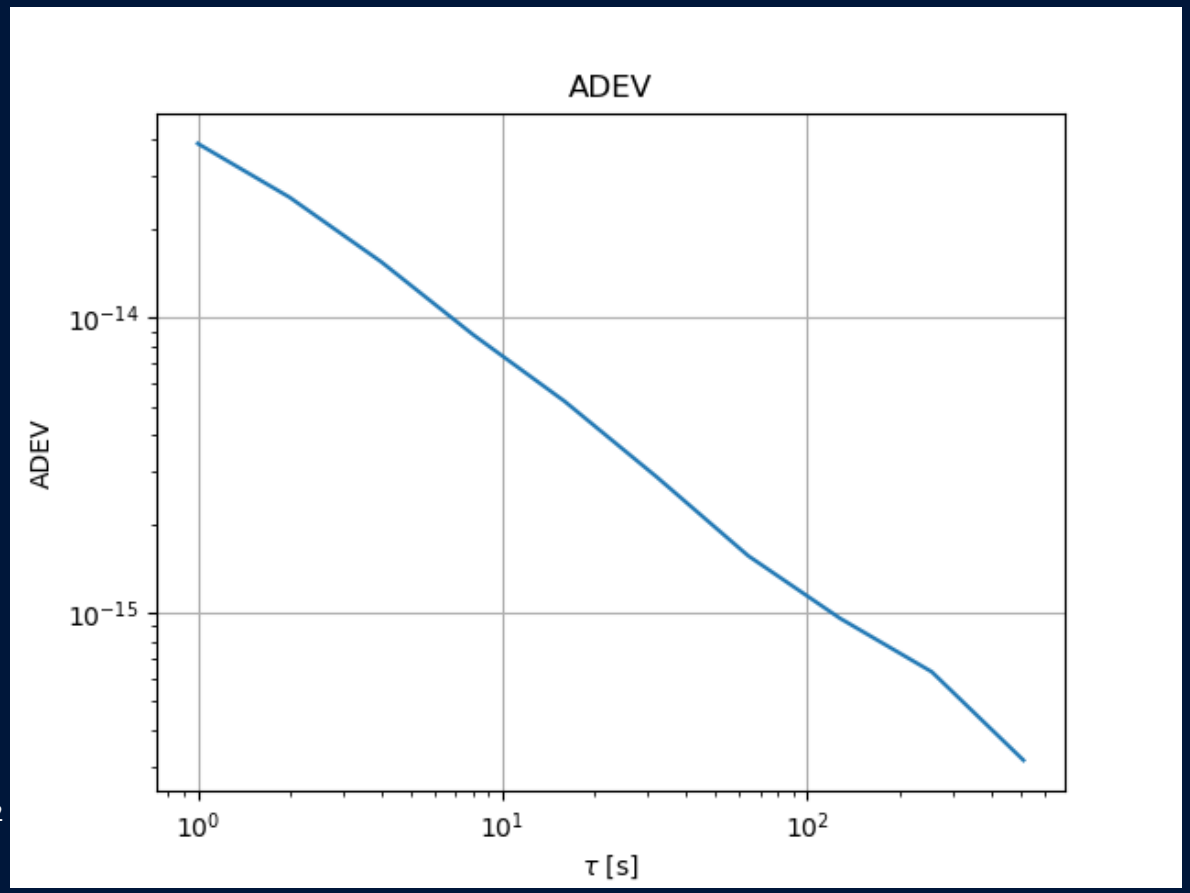
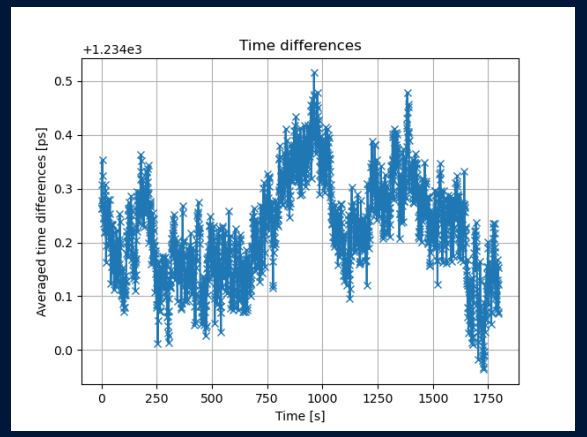
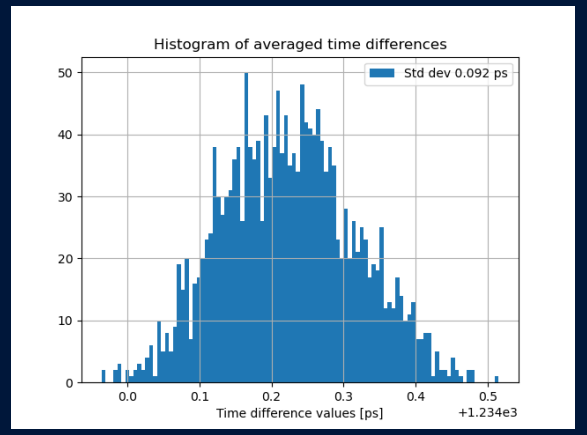
Verification examples

- Stability characterization of the time-difference measurement system: ADEV 4 x 10^{-14} at 1 s

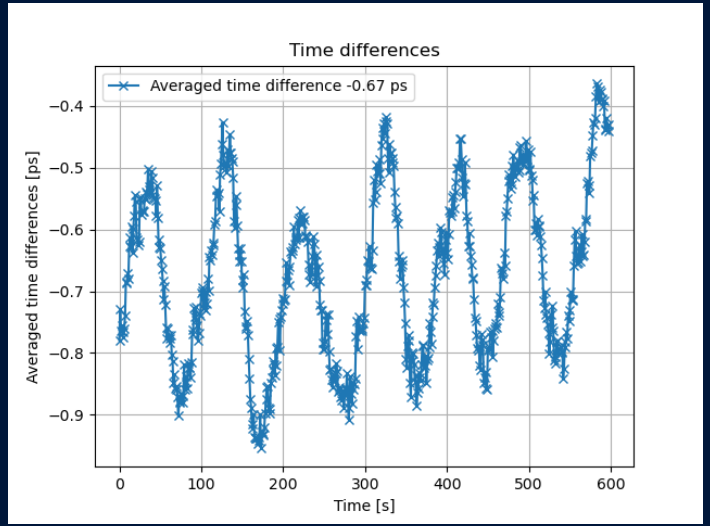




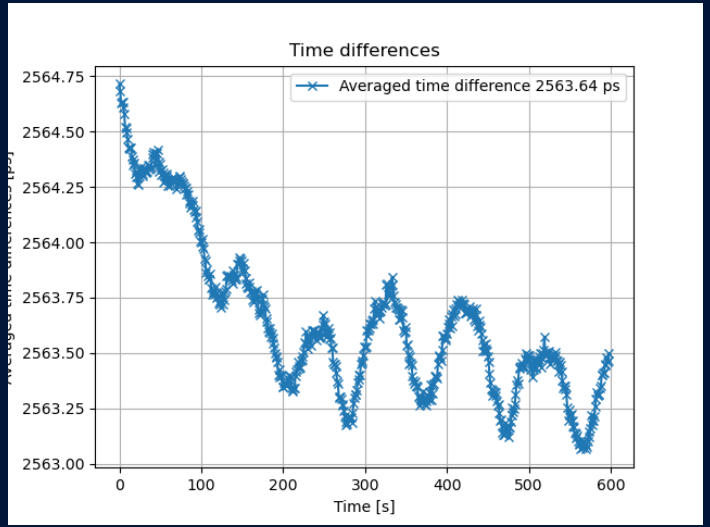


Verification examples

- Prolonged connection
  - Feeding two input channels from the same clock with the cables of the same length
  - Then changing length of one of these cables by 50 cm
  - Measuring the increase of the delay between channels
  - Theoretical increase: 2501 ps
    - Considering the signal propagation speed at 2/3 of speed of light
  - Measured increase: 2564 ps



Time difference for the same cables



Time difference for the cable extension

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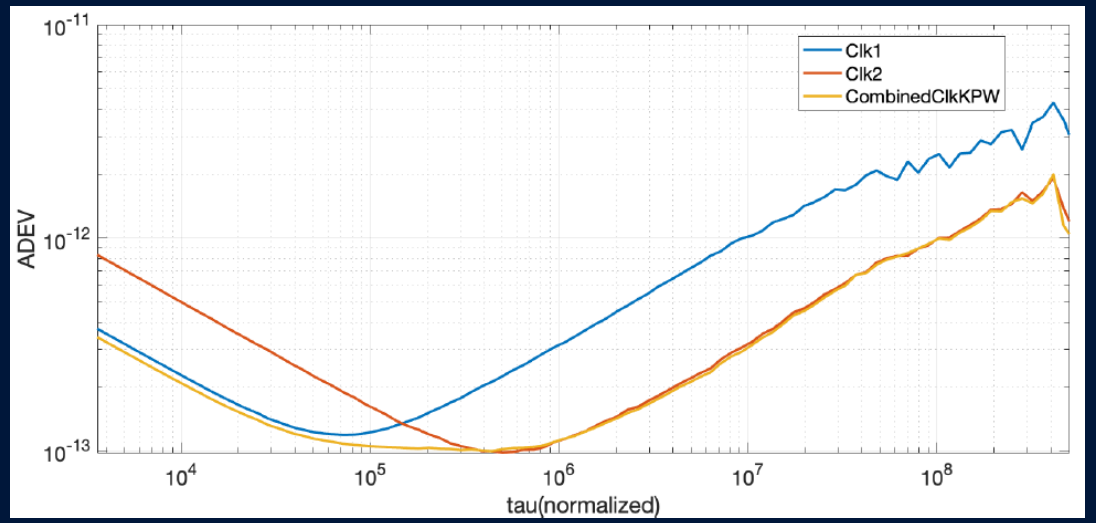
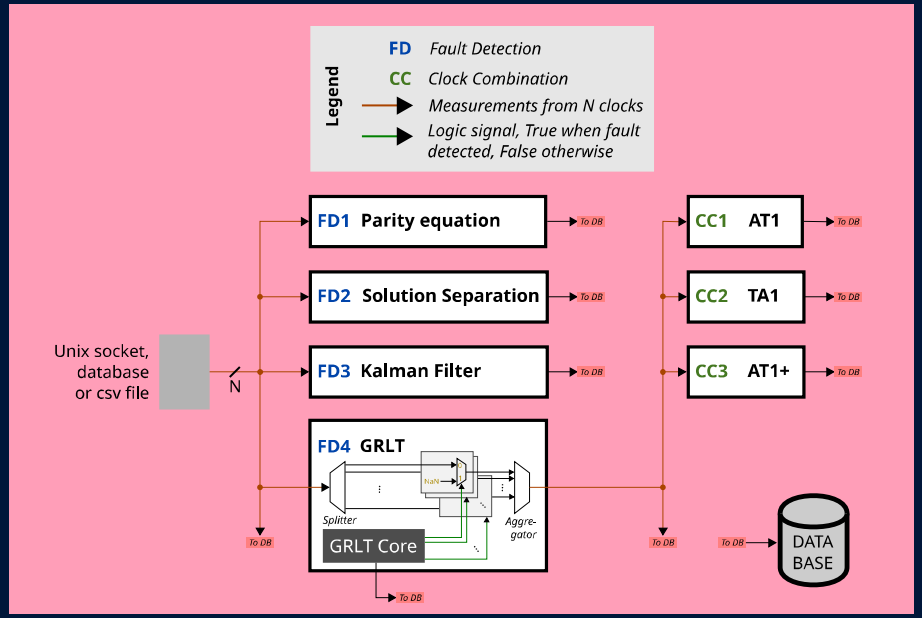
Algorithms

- Clock combination
  - Optimal ensemble of clocks leads to better frequency stability, and it is better than any of the individual clocks
  - Modern clock combination algorithms are based on Kalman filter (and state-space models)

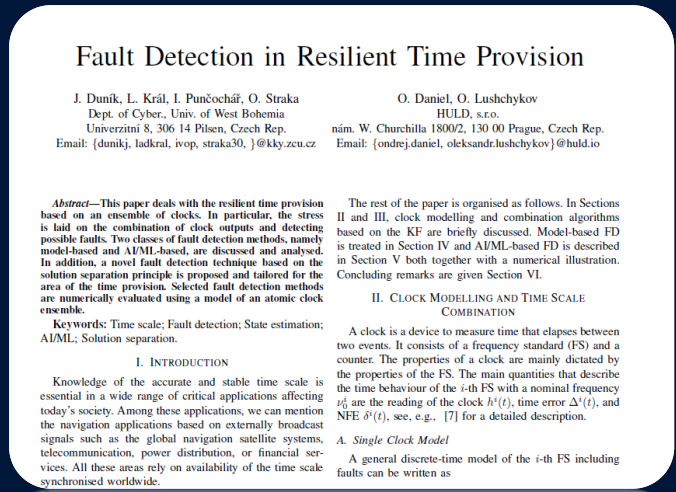


Algorithms

- Clock combination algorithms
  - AT1 [7]
  - AT1 + Kalman filter algorithm [8]
  - Pure Kalman filter algorithm (TA1) [9]
  - Stein algorithm [10]
- Fault detection algorithms
  - Generalized likelihood ratio test (GLRT)
  - Kalman filter innovation sequence monitor (ISM)
  - Parity equations (PE)
  - Solution separation (SolSep)
- Noise identification algorithms
  - Correlation approach
  - Allan variance approach



Interconnection of clock combination and fault detection algorithms



Fault Detection in Resilient Time Provision

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***Abstract*—This paper deals with the resilient time provision based on an ensemble of clocks. In particular, the stress is laid on the combination of clock outputs and detecting possible faults. Two classes of fault detection methods, namely model-based and AI/ML-based, are discussed and analysed. In addition, a novel fault detection technique based on the solution separation principle is proposed and tailored for the area of the time provision. Selected fault detection methods are numerically evaluated using a model of an atomic clock ensemble.**

Keywords: Time scale; Fault detection; State estimation; AI/ML; Solution separation.

I. Introduction

Knowledge of the accurate and stable time scale is essential in a wide range of critical applications affecting today's society. Among these applications, we can mention the navigation applications based on externally broadcast signals such as the global navigation satellite systems, telecommunication, power distribution, or financial services. All these areas rely on availability of the time scale synchronised worldwide.

The rest of the paper is organised as follows. In Sections II and III, clock modelling and combination algorithms based on the KF are briefly discussed. Model-based FD is treated in Section IV and AI/ML-based FD is described in Section V both together with a numerical illustration. Concluding remarks are given Section VI.

II. Clock Modelling and Time Scale Combination

A clock is a device to measure time that elapses between two events. It consists of a frequency standard (FS) and a counter. The properties of a clock are mainly dictated by the properties of the FS. The main quantities that describe the time behaviour of the i-th FS with a nominal frequency ν_0^i are the reading of the clock $h^i(t)$, time error $\Delta^i(t)$, and NFE $\delta^i(t)$, see, e.g., [7] for a detailed description.

A. Single Clock Model

A general discrete-time model of the i-th FS including faults can be written as

A paper on the **fault detection** published [11]

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Verification examples

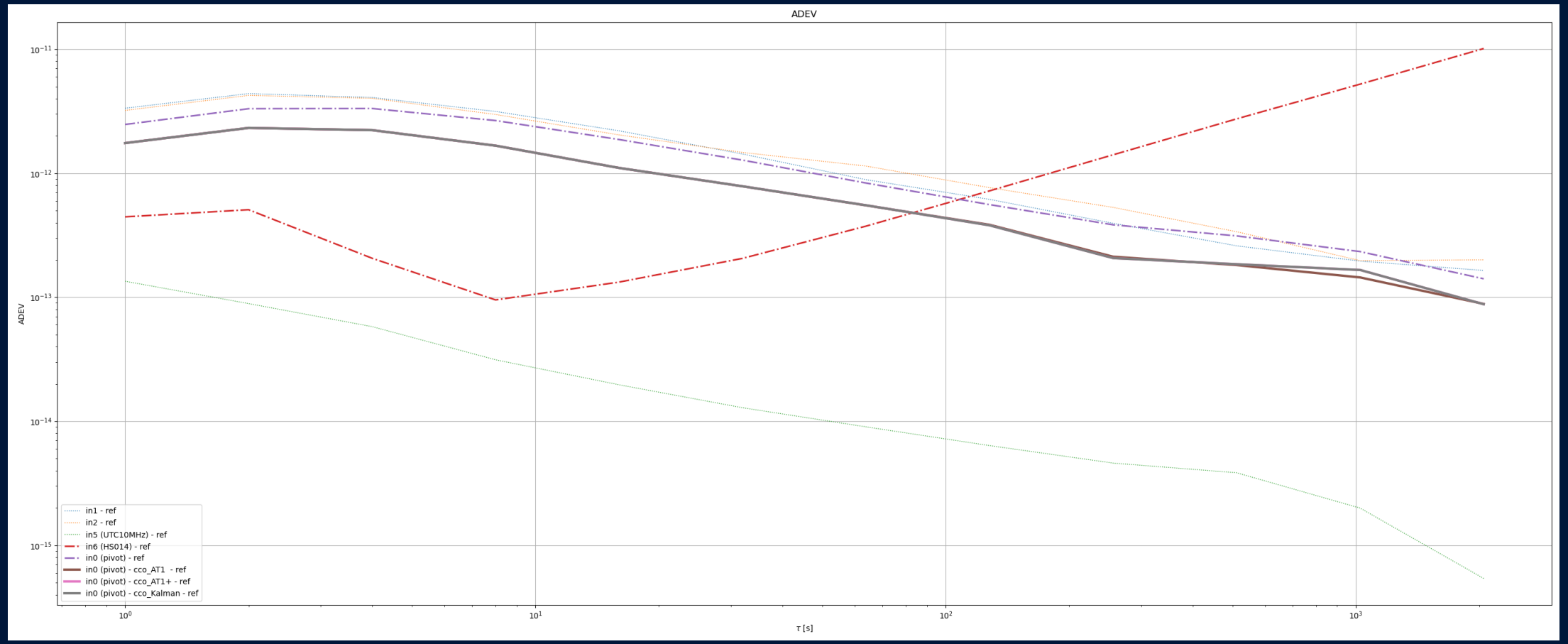
- Comparison of the ensemble and high-end atomic clock
  - Purpose: Demonstrate that the clock combination algorithms can generate the ensemble clock with superior stability with respect to the individual input clocks
  - Two variants:
    - Considering only cesium atomic clocks
    - Considering only hydrogen maser atomic clocks
- Steering HSO14 towards a maser clock
- Evaluation of fault detection algorithms
- All tests were performed in the ESA Timing Laboratory at ESTEC

Verification examples

- Comparison of the ensemble and high-end atomic clock
  - Cesium atomic clocks

ADC input	Clock type, *role*	Clock designator
0	Cesium, *pivot*	CS2
1	Cesium	CS3
2	Cesium	CS4
3	-	-
4	-	-
5	Maser	UTC-10MHz
6	OCXO	HSO14
7	Maser, *reference*	IM41

Input clock configuration

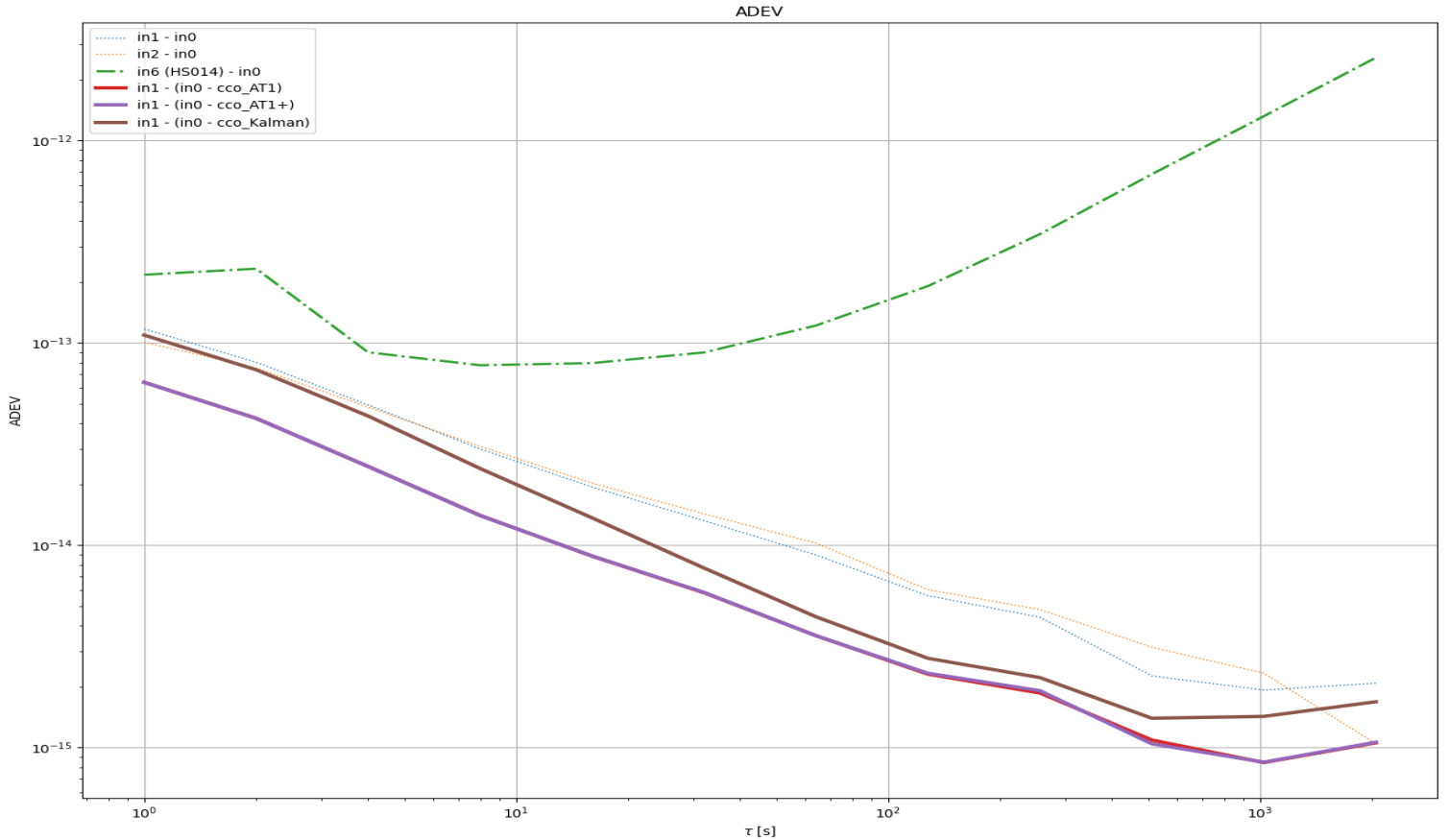


Verification examples

- Comparison of the ensemble and high-end atomic clock
  - Hydrogen maser clocks

ADC input	Clock type, *role*	Clock designator
0	Maser, *pivot and refence*	UTC-10MHz
1	Maser	IM41
2	Maser	IM43
3	-	-
4	-	-
5	-	-
6	OCXO	HSO14
7	-	-

Input clock configuration



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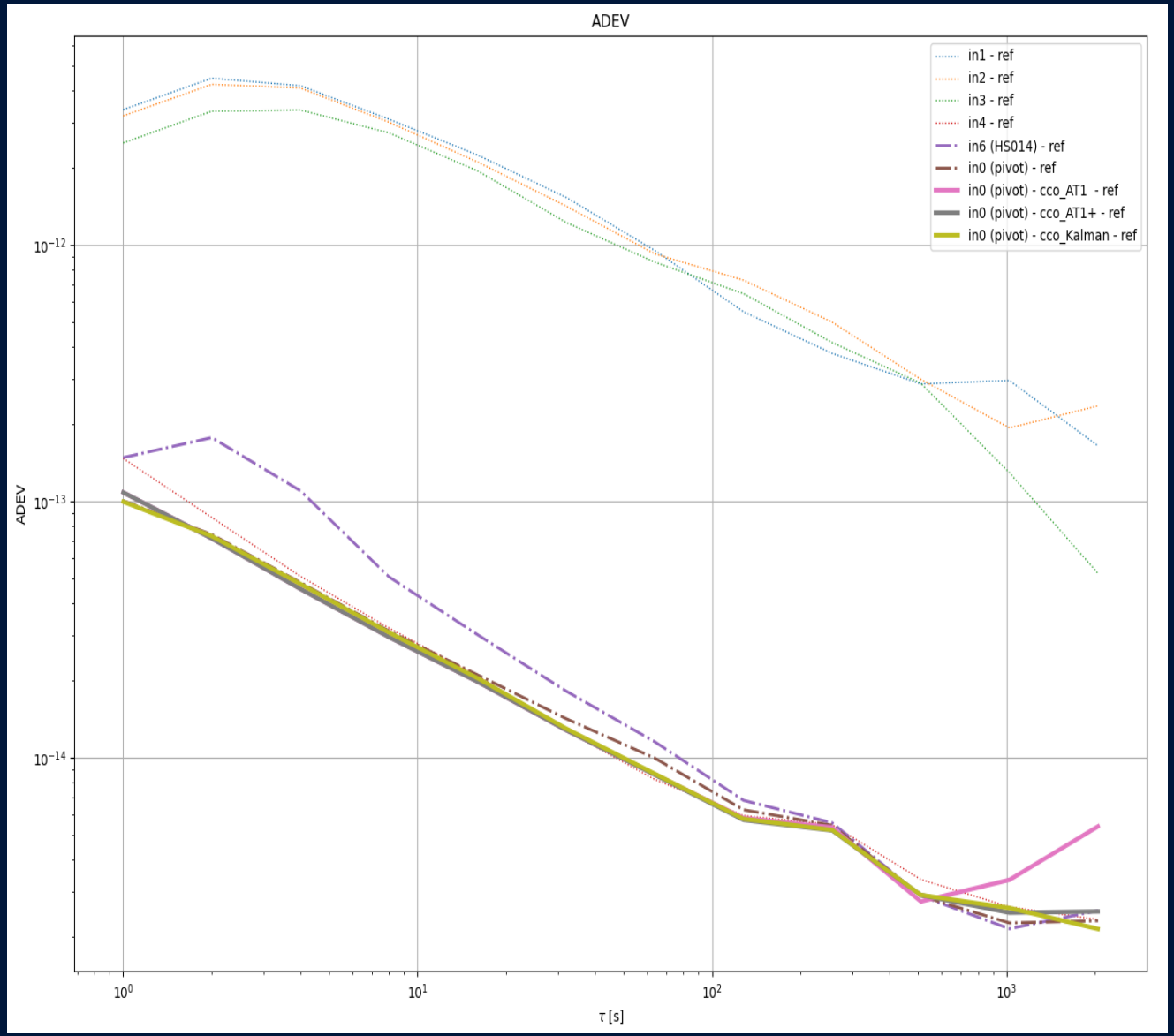
Verification examples

- Steering HSO14 towards a maser clock
- HSO14 *(denoted as "in6 (HSO14)-ref")* shall closely follow IM43 maser clock *(denoted as "in0 (pivot)-ref")*



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Verification example

- Evaluation of fault detection algorithms
  - Frequency jump

Fault magnitude	Fault duration [sec] (Start time – end time)	FD algorithms performance (fault detection and TTA [sec])			
		GLRT	ISM	PE	SolSep
10^{-10}	77 (15:11:00 - 15:12:27)	✓(<1)	✓(<1)	✓(<1)	✓(<1)
10^{-11}	77 (15:21:17 - 15:22:44)	✓(<1)	✓(<1)	✓(<2)	✓(<2)
10^{-12}	135 (15:30:00 - 15:32:15)	✓(<20)	×	×	×
10^{-13}	260 (15:40:40 - 15:45:00)	× / ✓ Threshold not exceeded but statistics visually raised	×	×	×
10^{-14}	270 (15:50:30 - 15:55:00)	×	×	×	×

An example of real-time visualization

Verification example

- Evaluation of fault detection algorithms
  - Phase jump

Fault magnitude	Fault duration [sec] (Start time – end time)	FD algorithms performance (fault detection and TTA [sec])			
		GLRT	ISM	PE	SolSep
5000 ps	3 (16:25:17 - 16:25:20)	✓(<1)	✓(<1)	✓(<1)	✓(<1)
500 ps	6 (16:31:46 - 16:31:52)	✓(<1)	✓(<1)	✓(<1)	✓(<1)
50 ps	10 (16:37:28 - 16:31:38)	✓(<1)	✓(<1)	✓(<1)	✓(<1)
5 ps	8 (16:43:42 - 16:43:50)	✓(<1)	✓(<1)	✓(<1)	✓(<1)
0.5 ps	12 (16:48:53 - 16:49:05)	×	✓ Detection probably due to fortunate noise realization	×	×

An example of real-time visualization

Future improvements

- PPS measurement resolution
- AI/ML fault detection
- Detection of anomalies on the master clock
- “Plug and play” approach for the inputs
- Multiple frequency jump detectors (with averaging)
- Sensitivity of fault detection algorithms
- Online identification of the clock model parameters
- Vibration testing
- Thermal testing

- **Transformation from prototype towards a product**

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Benefits working with ESA

- ESA is setting the course for the future technologies and supporting EU industry development
- Connecting relevant businesses and individuals through organizing events and workshops
- Guidance from the top-notch professionals in the field
- Directing the development in the efficient path
- Support with testing developed system
- Support with technical data needed for the successful project execution

Thank you very much!

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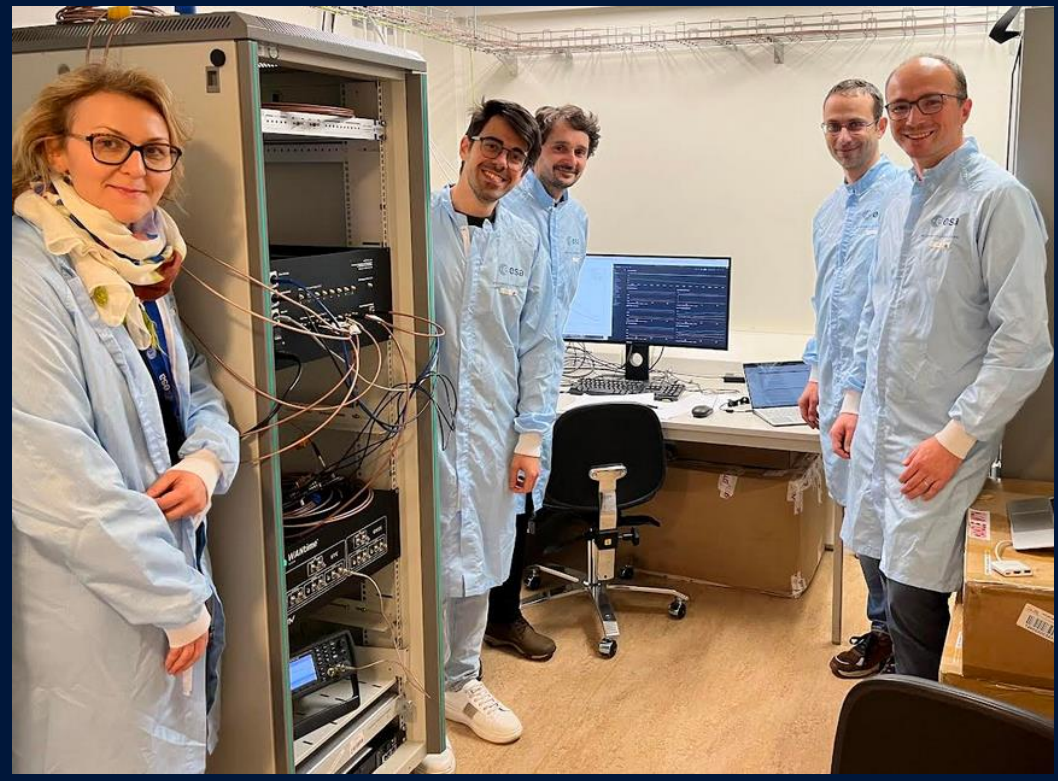

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Conclusion

- We developed a system capable of
  - Measuring time differences among input channels (at 10 MHz) with resolution of 0.1 ps
  - Running several clock combination algorithms in parallel
  - Steering a high stable oscillator towards an ensemble
- Moreover, the system can detect faults
  - Frequency errors at the level of 10^{-13}
  - Phase jumps down to 5 ps
- We developed supporting functions for identification of noise characteristics
- PPS subsystem currently at an inferior performance level
  - Shall be improved in relatively straightforward way
- The system was tested in ESA Timing Laboratory at ESTEC (November 2024) with positive results

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Beyond tomorrow

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